

# **Quasi Active High Power UHF Band Limiter Module**

#### **Features:**

Frequency Range: 300 MHz to 512 MHz

 High Average Power Handling: +56 dBm

 High Peak Power Handling: +56 dBm

Low Insertion Loss: < 0.4 dB

Return Loss: >18 dB

 Low Flat Leakage Power: <19 dBm

10.1mm x 6.2mm x 2.5mm SMT Module:

DC Coupling Capacitors

No external control lines or power supply required

RoHS Compliant

#### **Description:**

The RFLM-301511QC-392 SMT Silicon PIN Diode Limiter Module offers both High Power CW and Peak protection in the UHF Band region. It is based on proven hybrid assembly techniques utilized extensively in high reliability, mission critical applications. The RFLM-301511QC-392 offers excellent thermal characteristics in a compact, low profile 10mm x 6mm x 2.5mm package. The RFLM-301511QC-392 is designed for optimal small signal insertion loss permitting extremely low receiver noise figure while simultaneously offering excellent large input signal Flat Leakage for effective receiver protection in the UHF Band frequency range.

The limiter RF circuit characteristics provide outstanding passive receiver protection (Always On) which protects against High Average Power up to +56 dBm, High Peak Power up to +56 dBm pulsed, and maintains low flat leakage to less than +19 dBm.

#### ESD and Moisture Sensitivity Rating

The RFLM-301511QC-392 Limiter Module carries a Class 0 ESD rating (HBM) and an MSL 1 moisture rating.

#### Thermal Management Features

The RFLM-301511QC-392 base substrate has been designed to offer superior long term reliability in the customer's application by utilizing ultra-thin Au plating to combat Au embrittlement concerns. Also, a proprietary design methodology has minimized the thermal resistance from the PIN Diode junction to base plate. The two stage limiter design employs a second stage Schottky and quarter wavelength spacer detector circuit which permits ultra-fast turn on of the High Power PIN Diodes. This circuit topology coupled with the thermal

characteristic of the substrate design enables reliably handling High Input RF Power up to +56 dBm CW and RF Peak Power levels up to +56 dBm (20 ms pulse width @ 40% duty cycle with base plate temperature at 75°C).

## **Absolute Maximum Ratings**

@ Zo=50 $\Omega$ , T<sub>A</sub>= +25°C as measured on the base ground surface of the device.

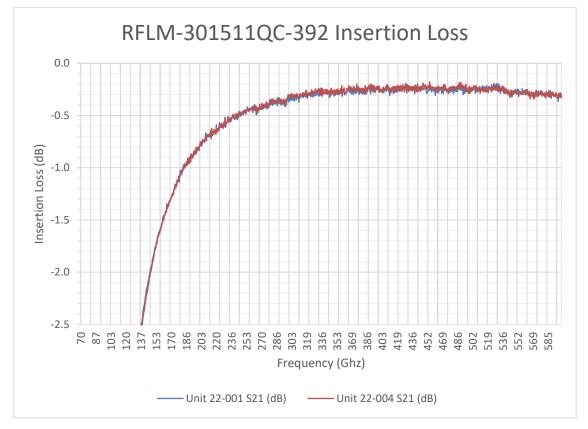
Parameter	Conditions	Absolute Maximum Value
Operating Temperature		-65°C to 125°C
Storage Temperature		-65°C to 150°C
Junction Temperature		175°C
Assembly Temperature	T = 30 seconds	260°C
RF Peak Incident Power	T <sub>CASE</sub> =75°C, source and load VSWR < 1.2, RF Pulse width = 20 msec, duty cycle = 40%, derated linearly to 0 W at T <sub>CASE</sub> =150°C (See note 1)	+56 dBm
RF CW Incident Power		+56 dBm
RF Input & Output DC Block Capacitor Voltage Breakdown		100 V DC
Thermal Resistance θ <sub>JC</sub>	Junction to bottom of package	24.5 °C/W

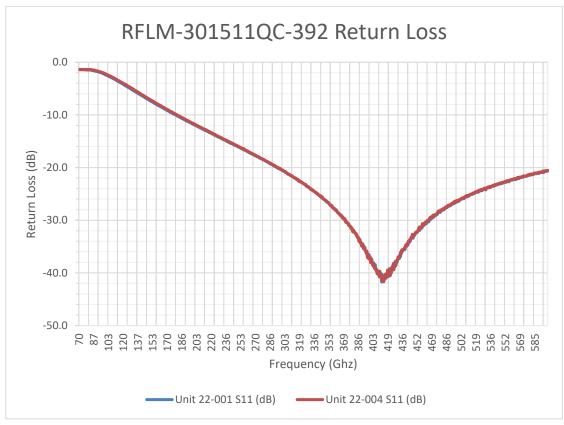
Note 1:  $T_{CASE}$  is defined as the temperature of the bottom ground surface of the device.

# **RFLM-301511QC-392 Electrical Specifications**

@ Zo=50 $\Omega$ , TA= +25°C as measured on the base ground surface of the device.

Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Frequency	F	300 MHz ≤ F ≤ 512 MHz	300		512	MHz
Insertion Loss	IL	$P_{in}$ = -20 dBm, $F = 300 - 512$ MHz		0.4	0.7	dB
Insertion Loss Rate of Change vs Operating Temperature	ΔIL	300 MHz ≤ F ≤ 512 MHz, Pin ≤ -20 dBm		0.005		dB/°C
Return Loss	RL	Pin= -20 dBm, F = 300 - 512 MHz	18			dB
Input 1 dB Compression Point	IP <sub>1dB</sub>	300 MHz ≤ F ≤ 512 MHz		12		dBm
2 <sup>nd</sup> Harmonic	2F <sub>o</sub>	$P_{in}$ = 0 dBm, $F_{o}$ = 512 MHz		-45		dBc
Peak Incident Power	P <sub>inc (PK)</sub>	RF Pulse = 20 msec, duty cycle = $40\%$ , $t_{rise} \le 2us$ , $t_{fall} \le 2$ usec			56	dBm
CW Incident Power	P <sub>inc(CW)</sub>	300 MHz ≤ F ≤ 512 MHz			56	dBm
Flat Leakage	FL	$P_{in}$ = 56 dBm, RF Pulse width = 20 ms, duty cycle = 40%, $t_{rise}$ ≤ 2 us, $t_{fall}$ ≤ 2 us		19		dBm
Spike Leakage Power	SLP	Pin = 56 dBm, RF Pulse width = 20 ms, duty cycle = 40%		28		dBm
Spike Leakage Energy	SLE	Pin = 56 dBm, RF Pulse width = 20 ms, duty cycle = 40%		0.5		erg
Recovery Time	T <sub>R</sub>	50% falling edge of RF Pulse to 1 dB IL, Pin = 56 dBm peak, RF PW = 20 ms, duty cycle = 40%, trise ≤ 2us, t <sub>fall</sub> ≤ 1 usec		7.5		usec



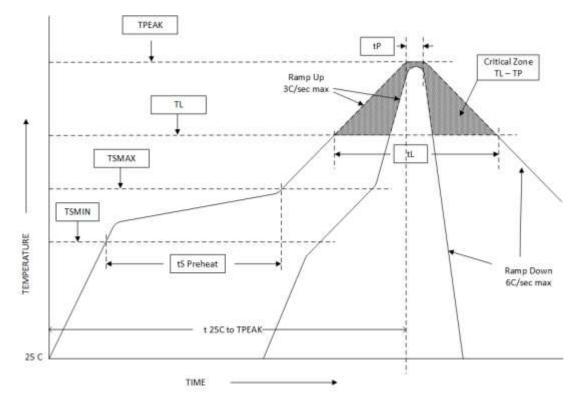


## **Assembly Instructions**

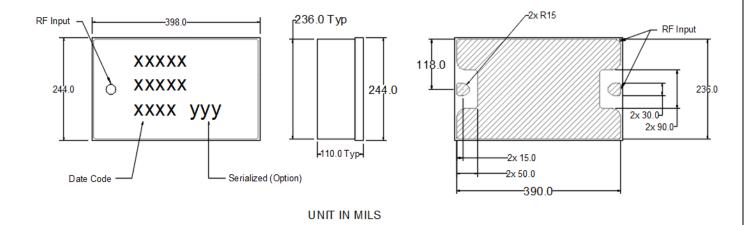
The RFLM-301511QC-392 may be attached to the printed circuit card using solder reflow procedures using either RoHS or Sn63/ Pb37 type solders per the Table and Temperature Profile Graph shown below:

Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate (T <sub>L</sub> to T <sub>P</sub> )	3°C/sec (max)	3°C/sec (max)
Preheat		
Temp Min (T <sub>smin</sub> )	100°C	100°C
Temp Max (T <sub>smax</sub> )	150°C	150°C
Time ( min to max) (t <sub>s</sub> )	60 – 120 sec	60 – 120 sec
$T_{smax}$ to $T_L$		
Ramp up Rate		3°C/sec (max)
Peak Temp (T <sub>P</sub> )	225°C +0°C / -5°C	260°C +0°C / -5°C
Time within 5°C of Actual Peak		
Temp (T <sub>P</sub> )	10 to 30 sec	20 to 40 sec
Time Maintained Above:		
Temp (T <sub>L</sub> )	183°C	217°C
Time (t <sub>L</sub> )	60 to 150 sec	60 to 150 sec
Ramp Down Rate	6°C/sec (max)	6°C/sec (max)
Time 25°C to T <sub>P</sub>	6 minutes (max)	8 minutes (max)

# **Solder Re-Flow Time-Temperature Profile**



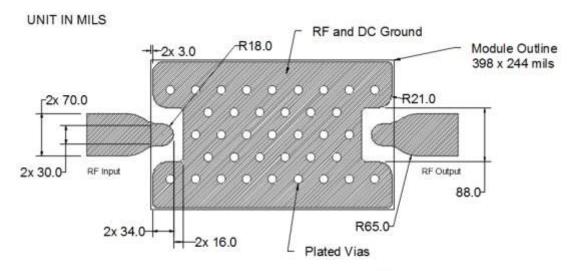
#### RFLM-301511QC-392 Limiter Module Package Outline Drawing



#### Notes:

- Metalized area on backside is the RF, DC and Thermal ground. In user's end application this surface temperature must be managed to meet the power handling requirements.
- 2) Back side metallization is thin Au termination plating to combat Au embrittlement (Au plated over Cu).

#### Recommended RFLM-301511QC-392 Solder Foot Print

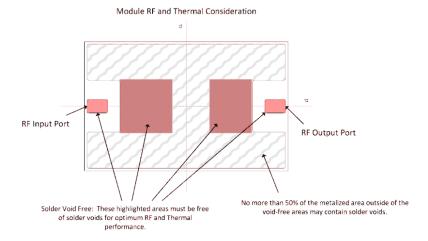


Low Signal PCB Layout Recommendation. Microstrip transmission line is based on Rogers 4003C, 32 mils, 1 oz copper. Minimum RF and DC ground illustrated. Plated vias are only sufficient for low signal evaluation. DXF available upon request.

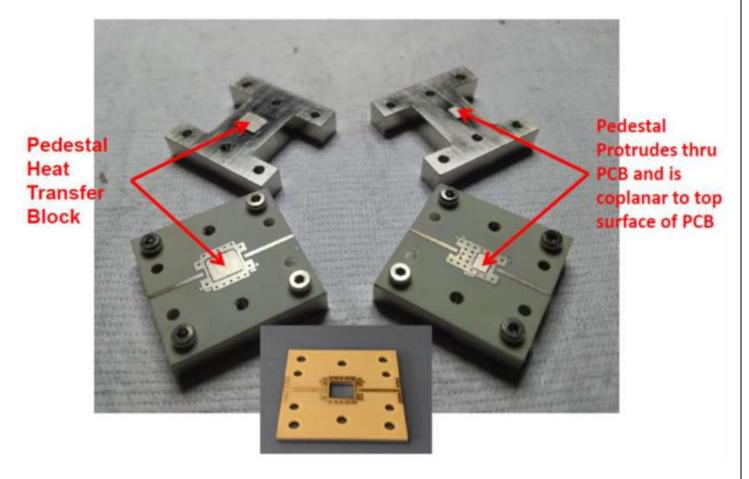
#### **Thermal Design Considerations:**

The design of the RFLM-301511QA-392 Limiter Module permits the maximum efficiency in thermal management of the PIN Diodes while maintaining extremely high reliability. Optimum Limiter performance and reliability of the device can be achieved by the maintaining the base ground surface temperature of less than 75°C.

There must be a minimal thermal and electrical resistance between the limiter bottom surface and ground. Adequate thermal management is required to maintain a T<sub>JC</sub> at less than +175°C and thereby avoid adversely affecting the semiconductor reliability. Special care must be taken to assure that minimal voiding occurs in the solder connection in the area shaded in red in the figure shown below:

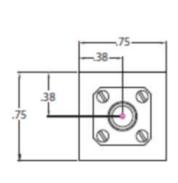


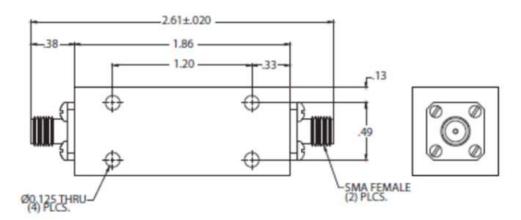
It is recommended that a low thermal impedance path be established between the base plate of the Limiter and the heat sink below. This can be achieved via the use of a copper embedded coin in the user's PCB design or via the use of a pedestal mounting technique (shown below) which permits a direct attachment of the Limiter's base plate to the heat sink below.



### **Connectorized Package Option**

The RFLM-301511QA-392 High Power IFF Limiter is available in a Connectorized Package with two female SMA connectors (input & output) and is denoted by the "C" suffix: RFLM-301511QA-392C. The RFLM-301511QA-392C includes both input and output DC Blocking capacitors. The packaged outline drawing is shown below:





# **Part Number Ordering Detail:**

The RFLM-301511QC-392 Limiter Module is available in the following format:

Part Number	Description	Packaging
RFLM-301511QC-392	UHF Band Limiter, Input & Output Blocking Caps	Gel-Pack
RFLM-301511QC-392 SS EVB	RFLM-301511QC-392 Small Signal Evaluation Board	Вох
RFLM-301511QC-392 HP EVB	RFLM-301511QC-392 High Power Evaluation Board	Вох
RFLM-301511QC-392C	RFLM-301511QC-392C SMA Connectorized Page Female-Female	Вох